A +2.4/0 V Controlled High Power GaAs SPDT Antenna Switch IC for GSM Application

Keiichi Numata, Yuji Takahashi, Tadashi Maeda, and Hikaru Hida

Photonic and Wireless Device Research Laboratories, NEC Corporation,
Tsukuba, Ibaraki 305-8501, JAPAN.

Abstract — **We have developed a high-power-handling and low-voltage-controlled GaAs single-pole dual-throw (SPDT) antenna switch for GSM application. The switch circuit configuration has a capacitor at the antenna terminal and two resistors between the transmitter (Tx) and receiver (Rx) terminals and the control terminals. This circuit enables the DC voltages of the Tx terminal and the Rx terminal to be separated from each other, resulting in a high-power-handling operation at a lower control voltage than that for the conventional switch. The developed SPDT switch demonstrated a handling power of 37.5 dBm and an insertion loss of 0.37 dB with a control voltage of +2.4/0 V.**

I. Introduction

Digital cellular-phone systems have been proliferating worldwide recently at a brisk pace. The development of advanced radio-frequency integrated circuits (RF ICs) to be used in the cellular handset has thus become increasingly important. Since most cellular-phone systems use time-division multiple access (TDMA), they usually have a transmitter and receiver (T/R) switch to connect the antenna to either the transmitting circuit or the receiving circuit. The RF output power from the power amplifier in a cellular handset is usually high, for example, 4 W for GSM, and the loss in the antenna switch must be compensated for by an increase in the output power from the power amplifier. Therefore, the antenna switch for these handsets must provide low insertion loss and high power-handling capability. Also, low voltage control is significantly becoming important. This is because the supply voltage of LSIs for the handsets has been decreased in order to reduce the amount of power they consume, and this has led to the use of low control voltages even for a switch IC. So far, a +3.0/0 V control antenna switch ICs has been developed [1]-[3]. However, as the control voltage of decreases to +2.4/0 V, the handling power also decreases in these conventional switch ICs.

This paper describes a developed antenna switch that uses a low control voltage. We have devised a novel configuration for the antenna switch so that it can produce high power for GSM applications at a low control voltage of +2.4/0 V without any degradation of performance of the switch.

II. Circuit Design

A. Antenna switch operation at low control voltage

Figure 1 shows a conventional single-pole dual-throw (SPDT) switch. This switch has two switch blocks, Tx and Rx, that have stacked FETs and resistors (Rg). This circuit operates as follows; two control signals, which are complementary, are applied to the control terminals of the Tx ($CONT_{(Tx)}$) and the Rx ($CONT_{(Rx)}$). When the voltage of $CONT_{(Tx)}$ is at a high level ($V_{c(on)}$) and $CONT_{(Rx)}$ is at a low level ($V_{c(off)}$), the Tx switch block is in a low-impedance state (on-state) and that of the Rx is in a high-impedance state (off-state).

To achieve high power-handling capability, the antenna switch usually has a stacked-FET configuration, as shown in Fig. 1. The maximum handling power of an antenna switch (Pmax) is determined as follows. Figure 2(a) shows an off-state switch block of n stacked FETs. An input signal swing (Vsw) is divided equally among the off-state FETs. Then the gate-source voltage and the gate-drain voltage of each FET are Vsw/2n. Figure 2(b) shows the Id-Vg curve and the swing level of the input signal, where V_{RF} is the DC voltage at the RF terminal, and Vt is

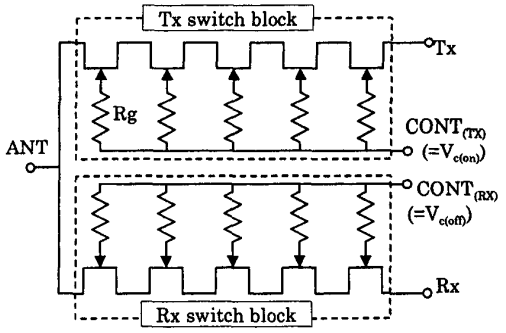

Figure 1. Schematic of conventional SPDT switch circuit.

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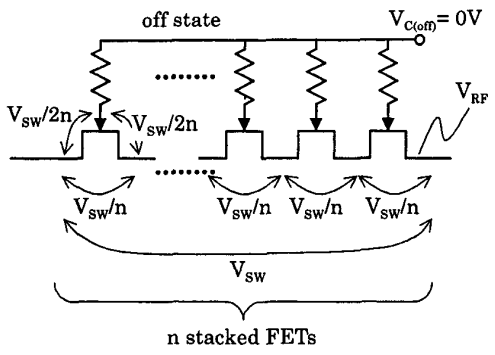
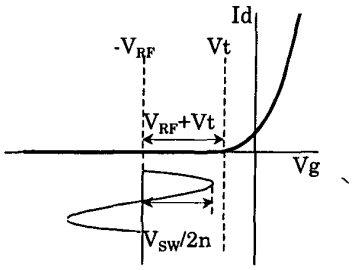


(a)



(b)

Figure 2. Applied voltage of off-state FETs. (a) Off-state switch block which contains n stacked FETs. (b) Id-Vg curve and the swing level of the input signal.

the threshold voltage of FETs. This figure shows that the FET can maintain its off-state until Vsw/2n is equal to V_{RF}+Vt; therefore, the maximum handling power of the switch IC (Pmax) is given by

$$Pmax=2\{n(V_{RF}+Vt)\}^2/Z_0, \qquad (1)$$

where Z_0 is the system impedance [2], [4]. In most cases, the V_{RF} of a conventional circuit, such as that shown in Fig. 1, settles about 0.3 V lower than $V_{c(on)}$ because Rg and the on-state FET generate a voltage drop. Therefore, increasing V_{RF} realizes an improved high handling-power capability at low control voltages.

However, insertion loss must also be taken into consideration when designing an antenna switch. The insertion loss of the antenna switch is given by

$$loss=20log\{2Z_0/(2Z_0+Zsw)\}, \qquad (2)$$

where Zsw is the impedance of the antenna switch. Zsw is determined by using the on-state resistance (Ron) and the

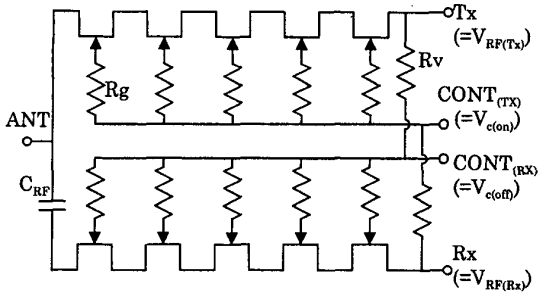


Figure 3. Schematic of the novel SPDT switch circuit.

off-state capacitance (Coff). In the range of the control voltage used in our experiments, Coff was hardly changed, thus, leading us to assume that Coff is constant. Hence, insertion loss can only be determined by using Ron, which is dependent on the applied voltage of an on-state FET, and is given as

$$Ron \propto n/\{Wg(V_{c(on)}-V_{RF}-Vt)\}, \qquad (3)$$

where Wg is the gate width of the FET.

Equation (3) indicates that an increase of V_{RF} to compensate for the degradation of the maximum handling power at a low control voltage is the cause of the increased insertion loss. That is a fundamental problem of a conventional antenna switch when handling a low control voltage. A novel circuit that can avoid these problems is described in the next section.

B. Proposal and design of novel switch circuit

Figure 3 shows a novel SPDT antenna switch. In this circuit, a capacitor (C_{RF}) is connected between the Rx switch block and the antenna terminal. This capacitor keeps the Tx and Rx DC voltages separate. This circuit also has two resistors (Rv) that are connected between $CONT_{(Rx)}$ and the Tx terminal, and $CONT_{(Tx)}$ and the Rx terminal. The resistance of Rv is chosen so that the DC voltage of the Tx terminal ($V_{RF(Tx)}$) is sufficiently low to reduce Ron, and the DC voltage of the Rx terminal ($V_{RF(Rx)}$) is sufficiently high to increase Pmax. As a result, the V_{RF} in the Eq. (1) and the V_{RF} in the Eq. (3) asymptotically approach $V_{c(on)}$ and $V_{c(on)}$-Vf, respectively. Here, Vf is gate turn-on voltage of FETs. Therefore the novel circuit enables high-handling-power operation and low insertion loss at a low control voltage.

Figure 4 shows Pmax as a function of V_{RF} at a Vt of –0.5 V. Here, the Pmax of the novel circuit is compared with that of the conventional circuit. This figure indicates that the Pmax of the conventional circuit with five stacked

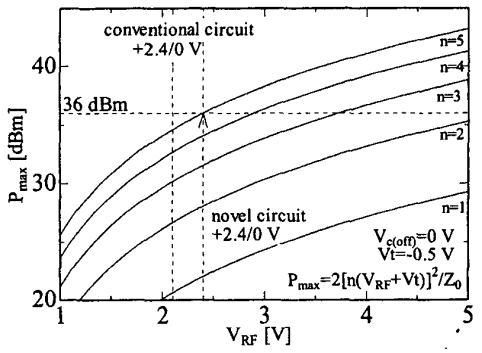


Figure 4. Power capability characteristics.

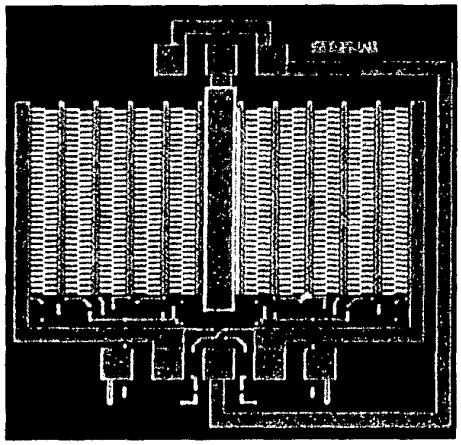


Figure 5. Microphotograph of developed IC.

FETs was below 36dBm at a control voltage of +2.4/0 V. However, in the novel circuit, since the DC voltage of the Rx settles approximately 2.4 V, a handling power of 36 dBm can be achieved with five stacked FETs.

Therefore, the problem previously described can be avoided without any degradation of performances in comparison with a conventional circuit at a low control voltage of +2.4/0 V.

III. Device Fabrication and Performances

SPDT switch ICs were fabricated using the GaAs heterojunction FET (HJFET) process [5]. An InGaAs channel, which has double-doped electron-supplying layers, was used to reduce Ron.

A microphotograph of the developed SPDT switch IC is shown in Fig. 5. The chip area is 1.3×1.2 mm, and this area is comparable to that of a conventional SPDT switch IC.

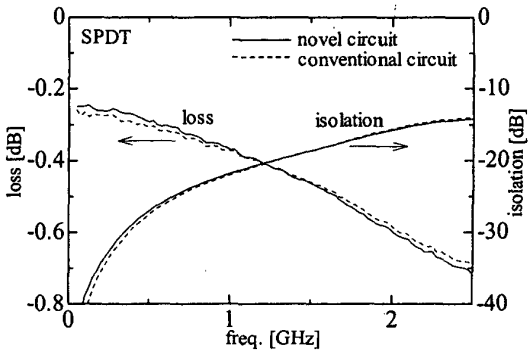


Figure 6. Comparison of frequency responses of the developed SPDT switch IC and conventional one.

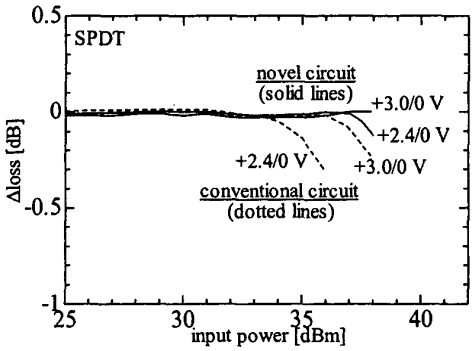


Figure 7. Comparison between power transfer characteristics of conventional and developed SPDT switch ICs.

The frequency responses of our novel circuit and a conventional circuit at the control voltage of +2.4/0 V are shown in Fig. 6. The insertion loss of the novel circuit is 0.37 dB and the isolation is −21.7 dB at 1 GHz. These performances are comparable to the characteristics of the conventional circuit.

Figure 7 shows the power transfer characteristics. Handling power $P_{-0.1dB}$ of the novel circuit is 37.5 dBm, which is an improvement of +3 dBm over the conventional circuit at a control voltage of +2.4/0 V; $P_{-0.1dB}$ with a control voltage of +3.0/0 V is over 38 dBm, which was limited by our measurement system.

Figure 8 shows the characteristics of the 2nd and 3rd-order harmonics. The harmonic characteristics are clearly correlated to handling power. Thus, the harmonics of the novel circuit are also improved compared to the conventional circuit. The 2nd and 3rd-order harmonics are −67.0 dBc and −80.4 dBc, respectively, at an input power of 36 dBm.

Figure 9 shows $P_{-0.1dB}$ of the novel circuit compared with P_{-1dB} of the conventional one [1], [6]. The curves shown

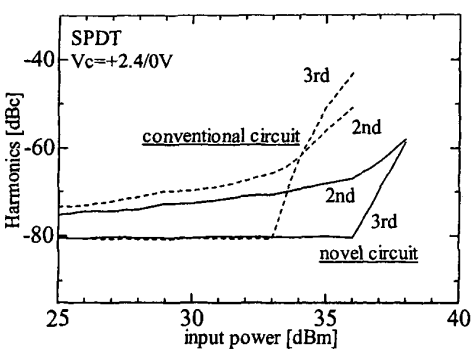


Figure 8. Comparison between harmonics characteristics of conventional and developed SPDT switch ICs

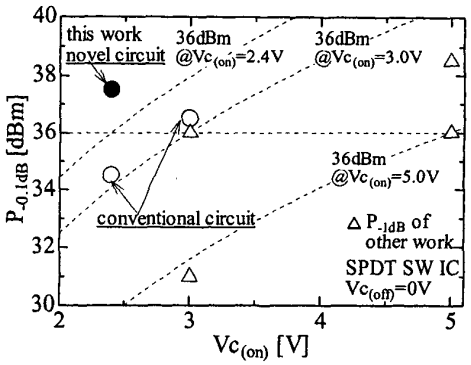


Figure 9.Comparison between handling power P_{-1dB} of previous switches and $P_{-0.1dB}$ of developed switch

TABLE I
CHARACTERISTICS OF FABRICATED SPDT SWITCH ICS AT +2.4/0 V CONTROL

	insertion loss		isolation		$P_{-0.1dB}$	Harmonics (at 36 dBm)	
	1 GHz	2 GHz	1 GHz	2 GHz		2f0	3f0
novel circuit	0.37 dB	0.59 dB	-21.7 dB	-15.7 dB	37.5 dBm	-67.0 dBc	-80.4 dBc
conventional circuit	0.37 dB	0.58 dB	-21.8 dB	-15.5 dB	34.5 dBm	-50.9 dBc	-42.9 dBc

in the figure were calculated from Eq. (1) to satisfy the handling power of 36 dBm at control voltages of 5, 3, and 2.4 V. This figure shows that the novel circuit can produce a very high handling-power capability. The performances of the fabricated ICs are summarized in Table I.

IV. CONCLUSION

A GaAs SPDT switch IC that operates +2.4/0 V using a novel circuit configuration was developed. This circuit configuration enables a high-handling-power operation at a low control voltage. The developed switch IC demonstrated a handling power of 37.5 dBm and an insertion loss of 0.37 dB with a control voltage of +2.4/0 V. This performance is sufficient for GSM application.

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